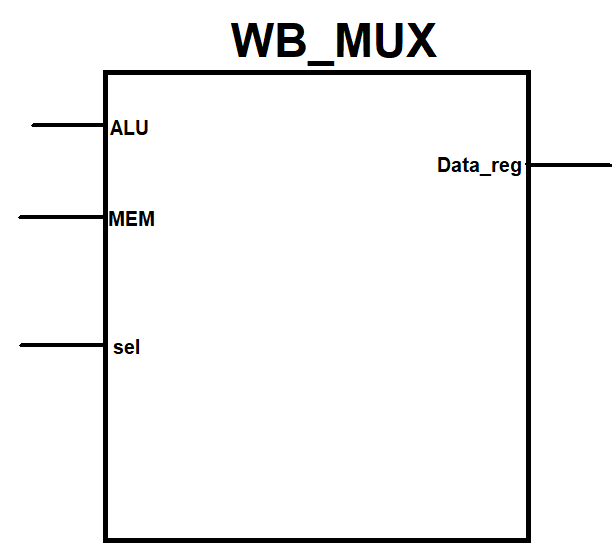
**99.WB\_MUX**

* Black-Box:



* Entity/Module Ports:  
    
  inputs:

sel – it selects between the inputs.

MEM – 32[Bits] this input comes from the memory.  
ALU – 32[Bits] this input comes from the ALU.

Outputs:

Data\_reg – 32[Bits] this output goes to the register file

* Architecture Description:

The module selects between 2 inputs that comes from the ALU and the memory and put it in the register file. .

* Target:

The module writing back the data to the register fetch .